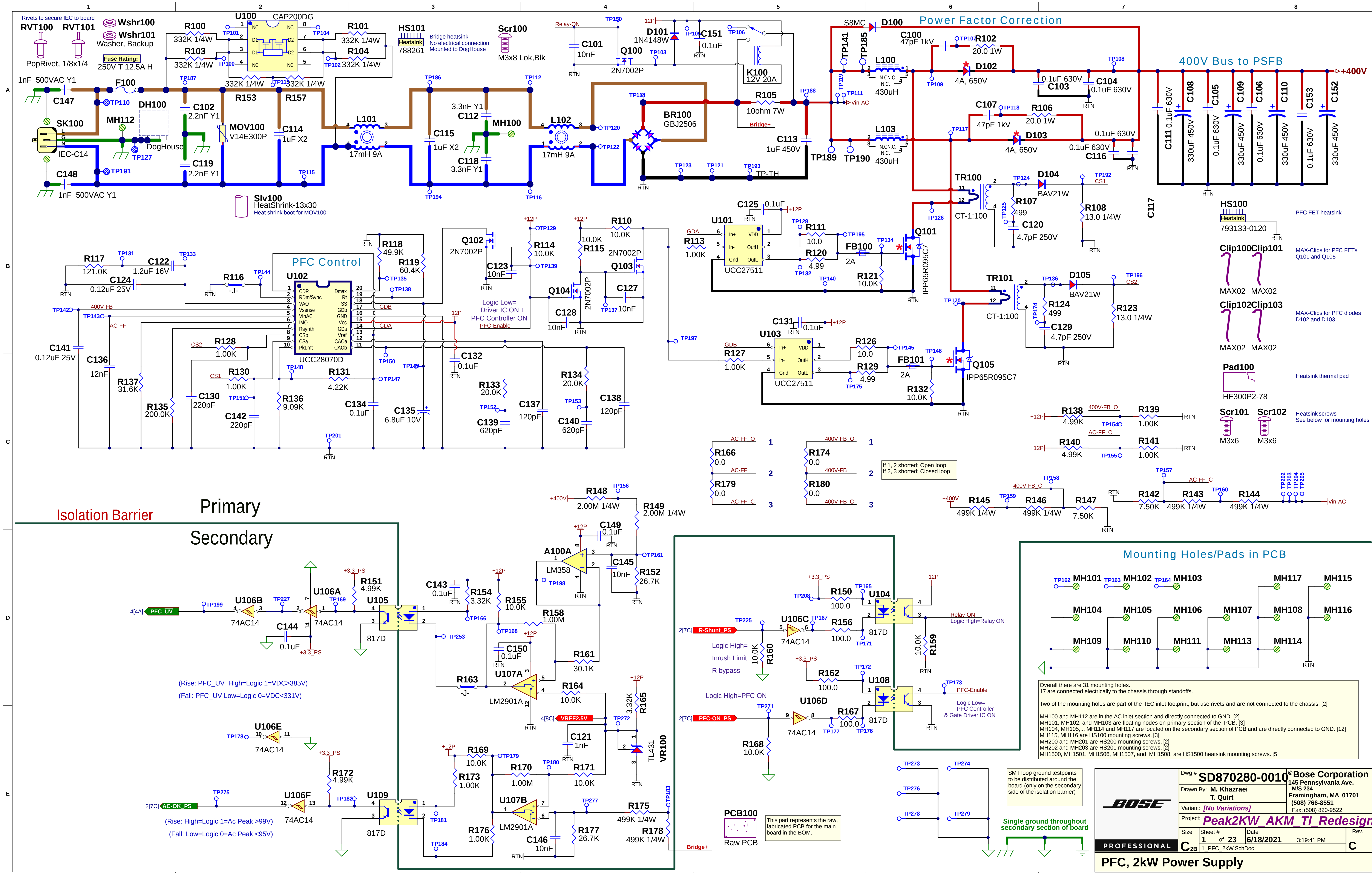

Power Factor Correction
400V Bus to PSFB
+400V
PFC Control
Primary
Secondary
Isolation Barrier
Mounting Holes/Pads in PCB
Rivets to secure IEC to board
RVT100 RVT101
PopRivet, 1/8x1/4
Wshr100
Wshr101
Washer, Backup
Fuse Rating:
250V T 12.5A H
HS101
Heatsink
788261
Bridge heatsink
No electrical connection
Mounted to DogHouse
Scr100
M3x8 Lok,Blk
Slv100
HeatShrink-13x30
Heat shrink boot for MOV100
HS100
793133-0120
PFC FET heatsink
Clip100 Clip101
MAX02 MAX02
MAX-Clips for PFC FETs
Q101 and Q105
Clip102 Clip103
MAX02 MAX02
MAX-Clips for PFC diodes
D102 and D103
Pad100
HF300P2-78
Heatsink thermal pad
Scr101 Scr102
M3x6 M3x6
Heatsink screws
See below for mounting holes
If 1, 2 shorted: Open loop
If 2, 3 shorted: Closed loop
Logic Low=
Driver IC ON +
PFC Controller ON
PFC-Enable
(Rise: PFC_UV High=Logic 1=VDC>385V)
(Fall: PFC_UV Low=Logic 0=VDC<331V)
(Rise: High=Logic 1=Ac Peak >99V)
(Fall: Low=Logic 0=Ac Peak <95V)
Logic High=
Inrush Limit
R bypass
Logic High=PFC ON
Relay-ON
Logic High=Relay ON
Logic Low=
PFC Controller
& Gate Driver IC ON
PCB100
Raw PCB
This part represents the raw, fabricated PCB for the main board in the BOM.
SMT loop ground testpoints to be distributed around the secondary side of the isolation barrier)
Single ground throughout secondary section of board
Overall there are 31 mounting holes.
17 are connected electrically to the chassis through standoffs.
Two of the mounting holes are part of the IEC inlet footprint, but use rivets and are not connected to the chassis. [2]
MH100 and MH112 are in the AC inlet section and connected to GND. [2]
MH101, MH102, and MH103 are floating nodes on primary section of the PCB. [3]
MH104, MH105,.., MH114 and MH117 are located on the secondary section of PCB and are directly connected to GND. [12]
MH115, MH116 are HS100 mounting screws. [3]
MH200 and MH201 are HS200 mounting screws. [2]
MH202 and MH203 are HS201 mounting screws. [2]
MH1500, MH1501, MH1506, MH1507, and MH1508, are HS1500 heatsink mounting screws. [5]
BOSE
PROFESSIONAL
Dwg # SD870280-0010
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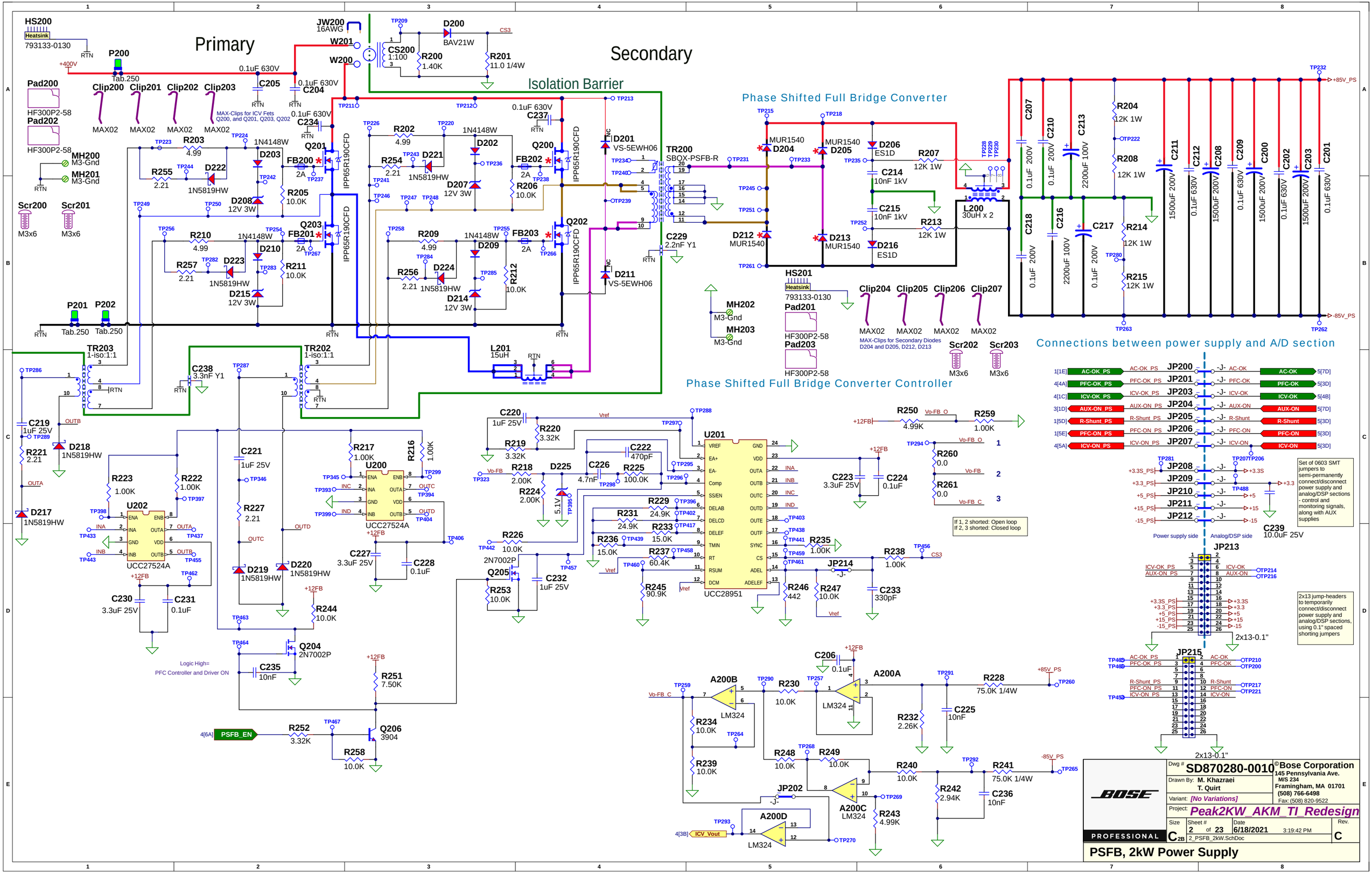
M/S 234
Framingham, MA 01701
(508) 766-8551
Fax: (508) 820-9522
Drawn By: M. Khazraei
T. Quirt
Variant: [No Variations]
Project: Peak2KW_AKM_TI_Redesign
Size C 2B
Sheet # 1 of 23
Date 6/18/2021 3:19:41 PM
1_PFC_2kW.SchDoc
Rev. C
PFC, 2kW Power Supply


Primary
Secondary
Isolation Barrier
Phase Shifted Full Bridge Converter
Phase Shifted Full Bridge Converter Controller
Connections between power supply and A/D section
HS200
Heatsink
793133-0130
P200
+400V
Tab.250
JW200
16AWG
W201
W200
CS200
1:100
R200
1.40K
D200
BAV21W
R201
11.0 1/4W
Pad200
HF300P2-58
Pad202
HF300P2-58
Clip200
Clip201
Clip202
Clip203
MAX02
MAX-Clips for ICV Fets
Q200, and Q201, Q203, Q202
C205
0.1uF 630V
C204
0.1uF 630V
C234
0.1uF 630V
C237
0.1uF 630V
MH200
M3-Gnd
MH201
M3-Gnd
Scr200
Scr201
M3x6
R203
4.99
R255
2.21
D203
1N4148W
D222
1N5819HW
D208
12V 3W
R205
10.0K
Q201
FB200
2A
IPP65R190CFD
R202
4.99
R254
2.21
D221
1N5819HW
D202
1N4148W
D207
12V 3W
R206
10.0K
Q200
FB202
2A
IPP65R190CFD
D201
VS-5EWH06
D211
VS-5EWH06
Q203
FB201
2A
IPP65R190CFD
R210
4.99
R257
2.21
D223
1N5819HW
D210
1N4148W
D215
12V 3W
R211
10.0K
R209
4.99
R256
2.21
D224
1N5819HW
D209
1N4148W
D214
12V 3W
R212
10.0K
Q202
FB203
2A
IPP65R190CFD
P201
P202
Tab.250
Tab.250
TR200
SBOX-PSFB-R
C229
2.2nF Y1
MUR1540
D204
MUR1540
D205
D212
MUR1540
D213
MUR1540
D206
ES1D
D216
ES1D
R207
12K 1W
C214
10nF 1kV
C215
10nF 1kV
R213
12K 1W
L200
30uH x 2
HS201
Heatsink
793133-0130
Pad201
HF300P2-58
Pad203
HF300P2-58
MH202
M3-Gnd
MH203
M3-Gnd
Clip204
Clip205
Clip206
Clip207
MAX02
MAX-Clips for Secondary Diodes
D204 and D205, D212, D213
Scr202
Scr203
M3x6
C207
C210
C213
C218
C216
C217
2200uF 100V
0.1uF 200V
1500uF 200V
0.1uF 630V
1500uF 200V
C211
C212
C208
C209
C200
C202
C203
C201
R204
12K 1W
R208
12K 1W
R214
12K 1W
R215
12K 1W
TP232
+85V_PS
-85V_PS
TP262
TP263
TP222
TP280
TR203
1-iso:1:1
TR202
1-iso:1:1
C238
3.3nF Y1
L201
15uH
C219
1uF 25V
D218
1N5819HW
R221
2.21
D217
1N5819HW
C221
1uF 25V
R227
2.21
D219
1N5819HW
D220
1N5819HW
R223
1.00K
R222
1.00K
U202
UCC27524A
R217
1.00K
R216
1.00K
U200
UCC27524A
C227
3.3uF 25V
C228
0.1uF
C230
3.3uF 25V
C231
0.1uF
R244
10.0K
Q204
2N7002P
C235
10nF
R251
7.50K
R252
3.32K
Q206
3904
R258
10.0K
PSFB_EN
Logic High=
PFC Controller and Driver ON
C220
1uF 25V
R220
3.32K
R219
3.32K
R218
2.00K
D225
5.1V
C222
470pF
C226
4.7nF
R225
100.0K
R226
10.0K
2N7002P
Q205
C232
1uF 25V
R253
10.0K
R229
24.9K
R231
24.9K
R233
15.0K
R236
15.0K
R237
60.4K
R245
90.9K
U201
UCC28951
R235
1.00K
R238
1.00K
JP214
-J-
R246
442
R247
10.0K
C233
330pF
C223
3.3uF 25V
C224
0.1uF
R250
4.99K
R259
1.00K
R260
0.0
R261
0.0
If 1, 2 shorted: Open loop
If 2, 3 shorted: Closed loop
C206
0.1uF
A200B
LM324
R230
10.0K
A200A
LM324
R228
75.0K 1/4W
C225
10nF
R232
2.26K
R234
10.0K
R239
10.0K
R248
10.0K
R249
10.0K
A200C
LM324
R240
10.0K
R241
75.0K 1/4W
C236
10nF
R242
2.94K
JP202
-J-
A200D
LM324
R243
4.99K
JP200
JP201
JP203
JP204
JP205
JP206
JP207
AC-OK_PS
PFC-OK_PS
ICV-OK_PS
AUX-ON_PS
R-Shunt_PS
PFC-ON_PS
ICV-ON_PS
Set of 0603 SMT jumpers to semi-permanently connect/disconnect power supply and analog/DSP sections - control and monitoring signals, along with AUX supplies
Power supply side
Analog/DSP side
JP208
JP209
JP210
JP211
JP212
C239
10.0uF 25V
JP213
2x13-0.1"
JP215
2x13-0.1"
2x13 jump-headers to temporarily connect/disconnect power supply and analog/DSP sections, using 0.1" spaced shorting jumpers
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Fax: (508) 820-9522
Dwg # SD870280-0010
Drawn By: M. Khazraei
T. Quirt
Variant: [No Variations]
Project: Peak2KW_AKM_TI_Redesign
Size C2B
Sheet # 2 of 23
Date 6/18/2021 3:19:42 PM
Rev. C
2_PSFB_2kW.SchDoc
PSFB, 2kW Power Supply
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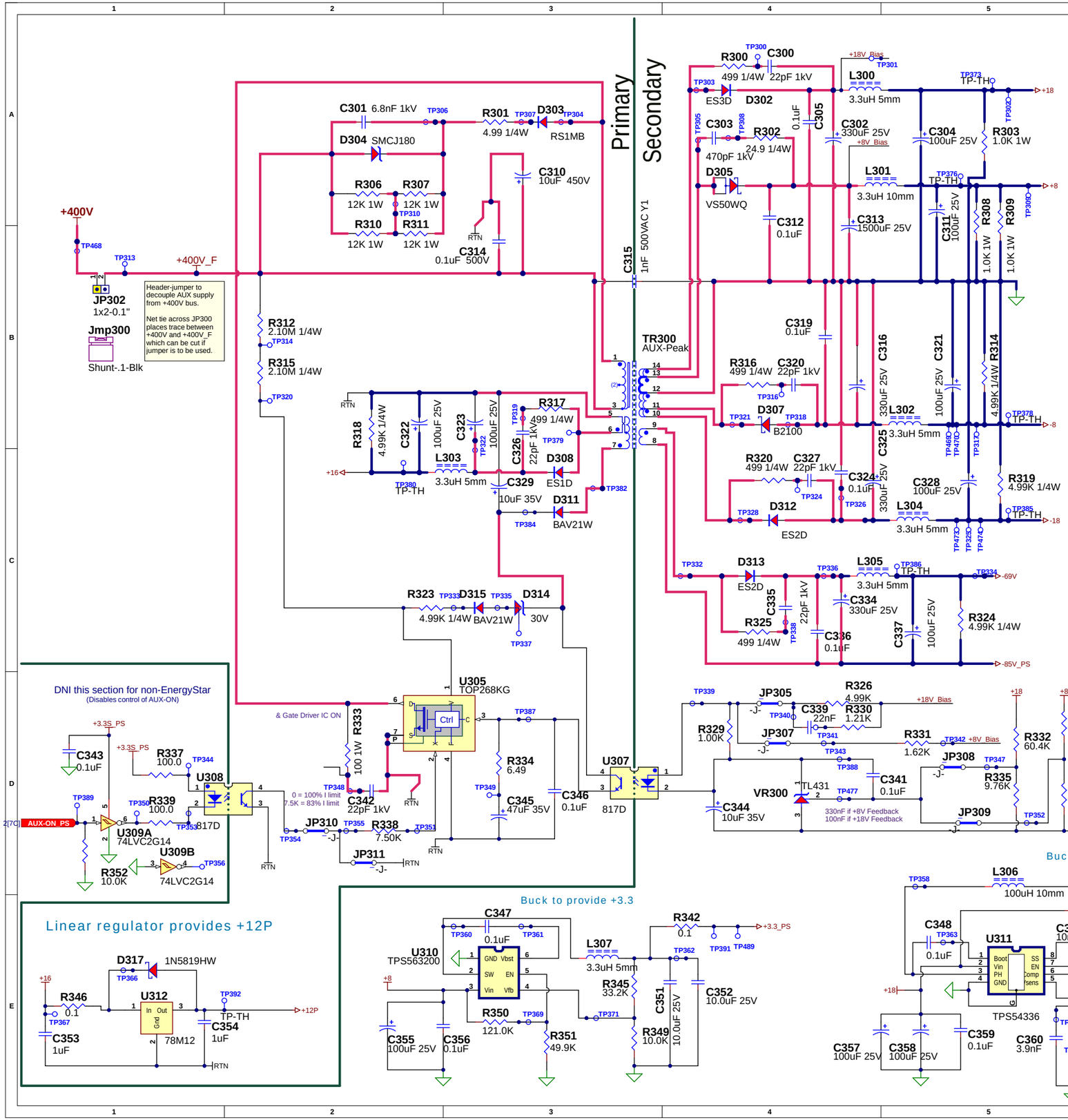

Dwg #	SD870280-0010
Drawn By:	M. Khazraei T. Quirt
Variant:	[No Variations]
Project:	Peak2KW_AKM_TI_Redesign
Size	C2B
Sheet #	3 of 23
Date	6/18/2021 3:19:42 PM
Rev.	C
	3_AuxPowerSupply_2kW.SchDoc

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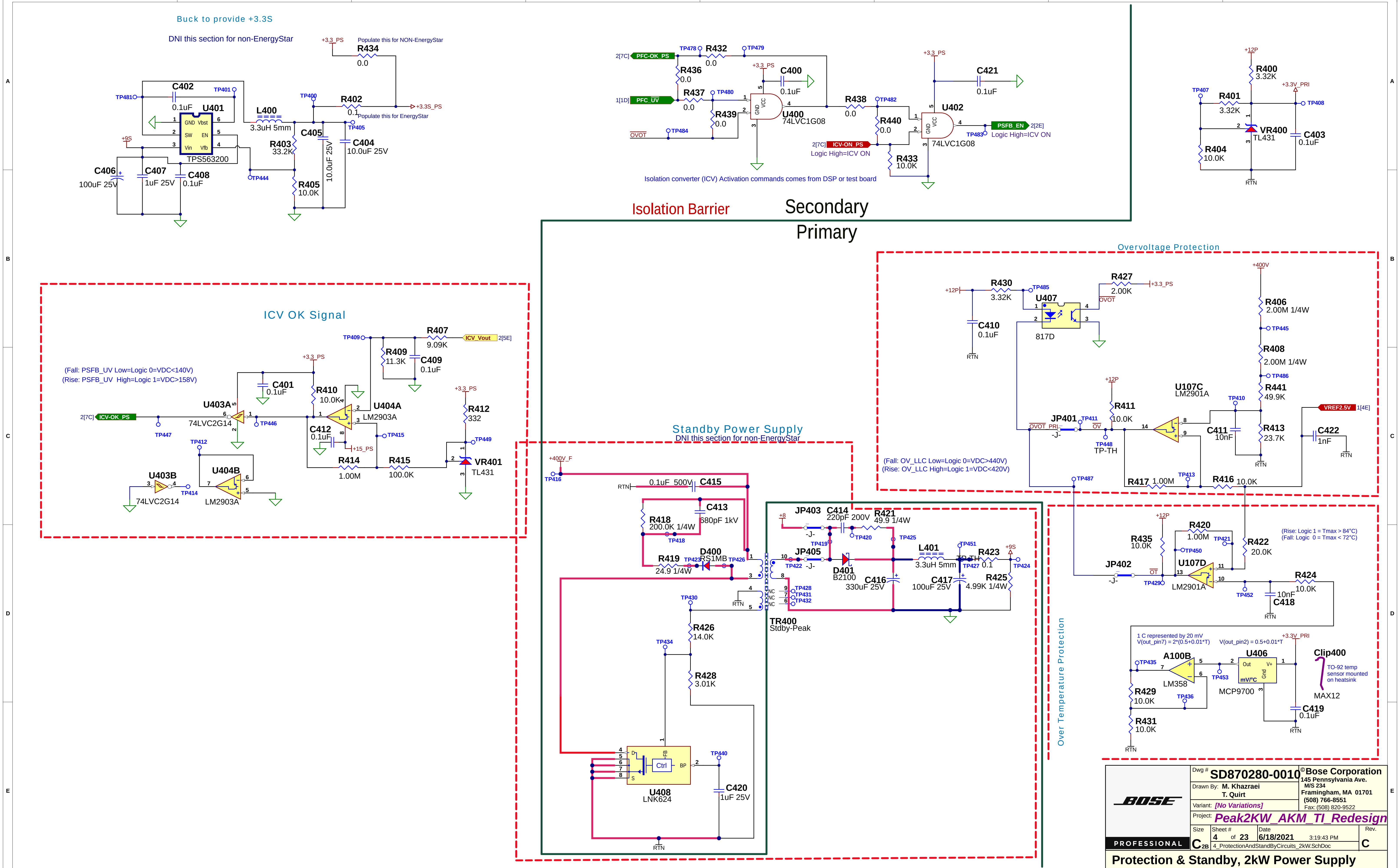
2kW Auxiliary Power Supply



Dwg # SD870280-0010

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Drawn By: M. Khazraei, T. Quirt

Variant: [No Variations]

Project: Peak2KW_AKM_TI_Redesign

Size C2B | Sheet # 4 of 23 | Date 6/18/2021 3:19:43 PM | Rev. C

4_ProtectionAndStandByCircuits_2kW.SchDoc

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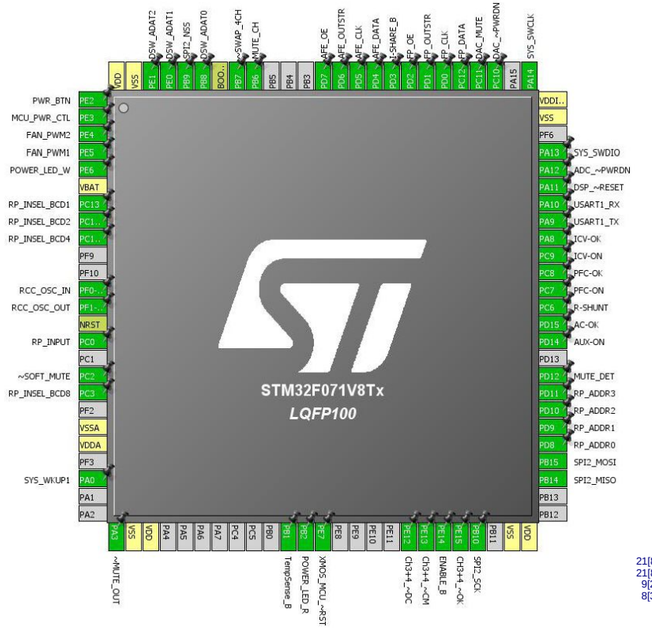
Protection & Standby, 2kW Power Supply



Note:

For 2-channel amps, Channels 3 & 4 are used. Common components are preserved.

Connections between MCU and amp are labeled as Amp B and Channels 3 & 4 for consistency with P2.

ARM Cortex-M0 microcontroller

SWD header

Debug UART

Debug GPIO

Dwg #	SD870280-0010
Drawn By:	B. Sennett, B. Zhao
Variant:	[No Variations]
Project:	Peak2KW_AKM_TI_Redesign
Size	C2B
Sheet #	5 of 23
Date	6/18/2021 3:19:43 PM
Rev.	C
	5_Micro.SchDoc

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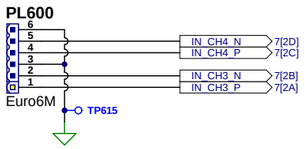
Microcontroller



Note:

For 2-channel amps, Channels 3 & 4 are used. Common components are preserved.

The input connector PL600 appears on this page but the remaining AFE circuits are located on Page 7.

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Dwg # SD870280-0010

Drawn By: B. Sennett
B. Zhao

Variant: *[No Variations]*

Project: *Peak2KW_AKM_TI_Redesign*

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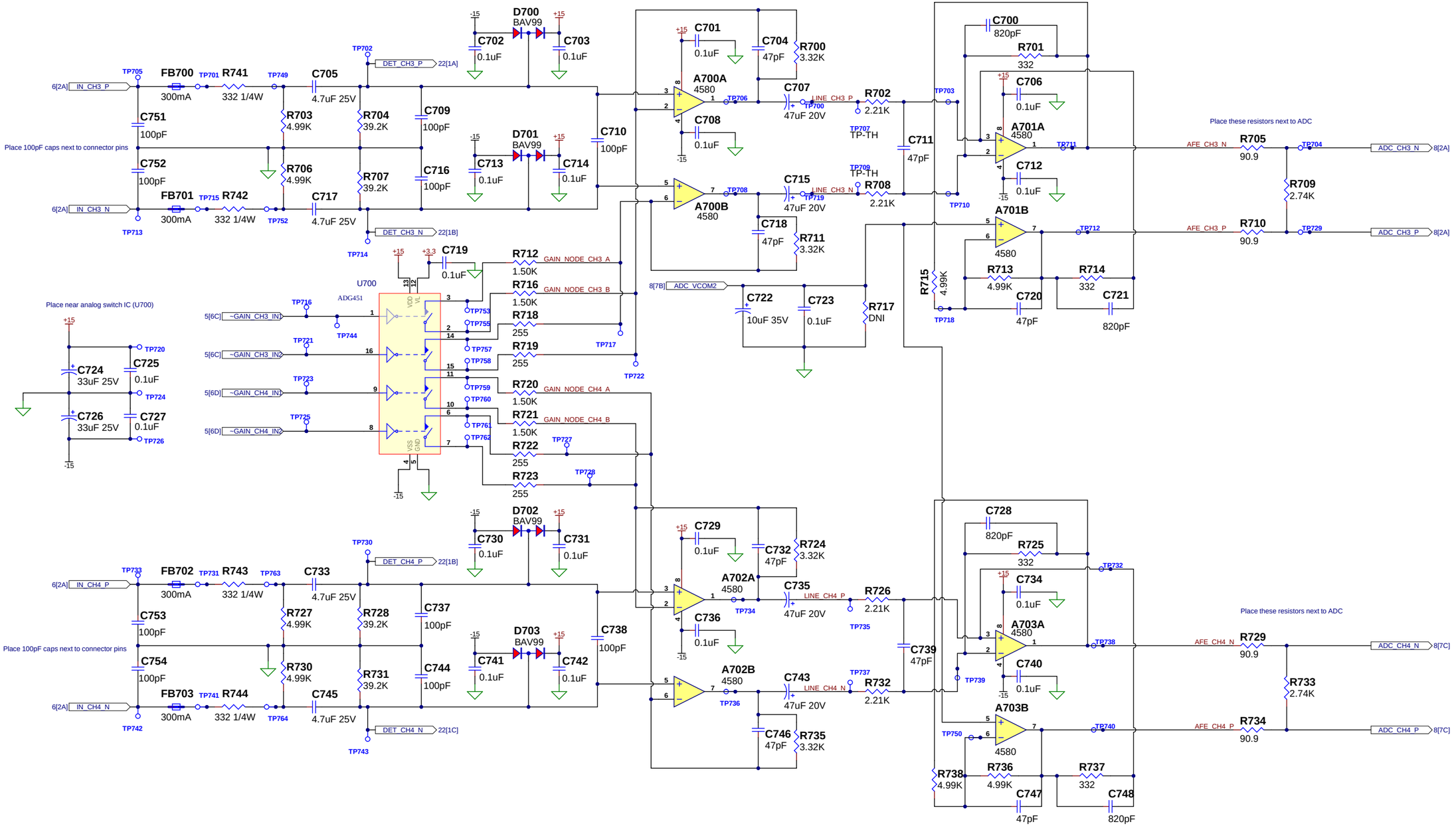
Size C2B | Sheet # 6 of 23 | Date 6/18/2021 3:19:43 PM | Rev. C

6_AFE12.SchDoc

Analog Front-End Ch. 1 & 2



Dwg #	SD870280-0010
Drawn By:	B. Sennett B. Zhao
Variant:	[No Variations]
Project:	Peak2KW_AKM_TI_Redesign
Size	C2B
Sheet #	7 of 23
Date	6/18/2021 3:19:44 PM
File	7_AFE34.SchDoc
Rev.	C

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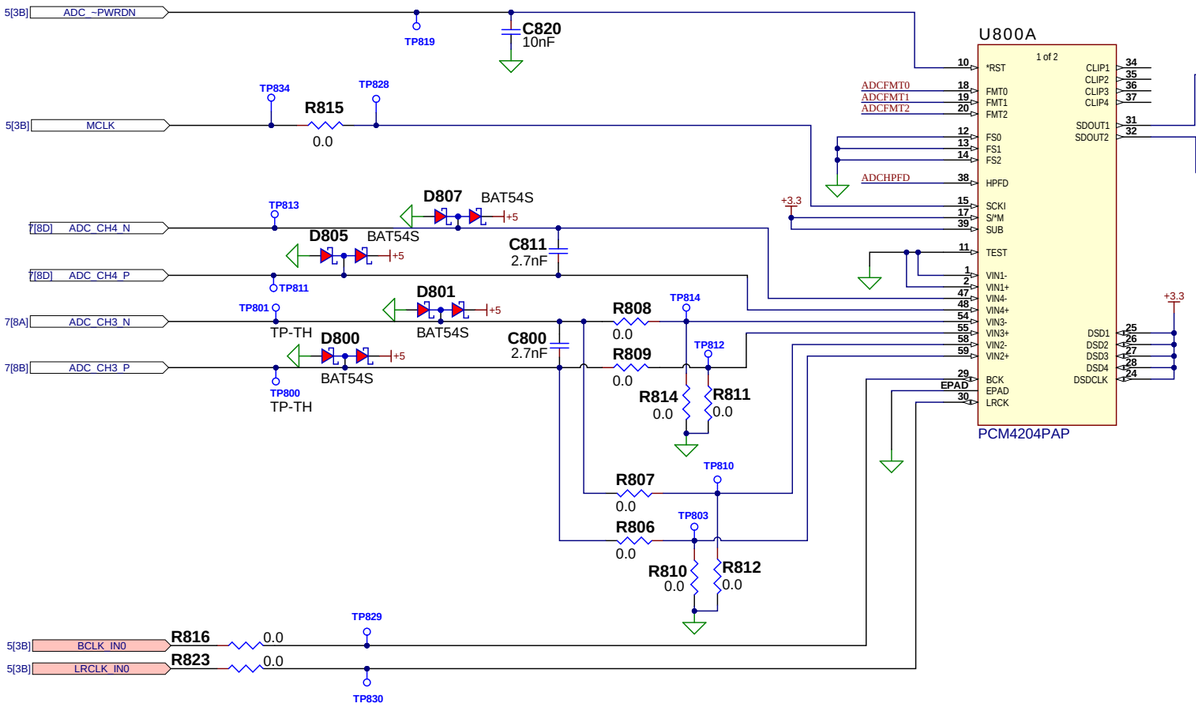
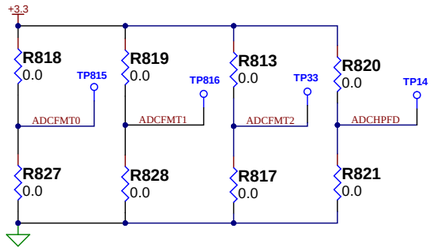
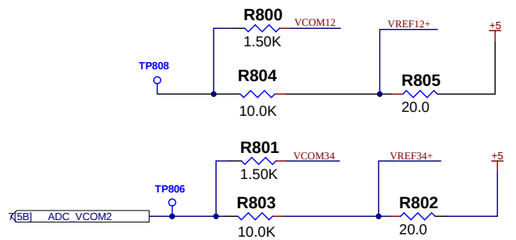
Analog Front-End Ch. 3 & 4

ADC Option Configuration

ADC Pin	Signal Name	Setting	Configuration
12	FS0	LOW	Single rate with clock auto-detection (Fs = 48 KHz, SCKI = 512Fs = 24.576 MHz)
13	FS1	LOW	
14	FS2	LOW	
17	S/*M	HIGH	Slave mode
18	FMT0	LOW	24-bit left-justified
19	FMT1	LOW	
20	FMT2	LOW	
38	HPFD	HIGH	Internal high-pass filter disabled
39	SUB	HIGH	TDM sub-frame 1 (N/A)

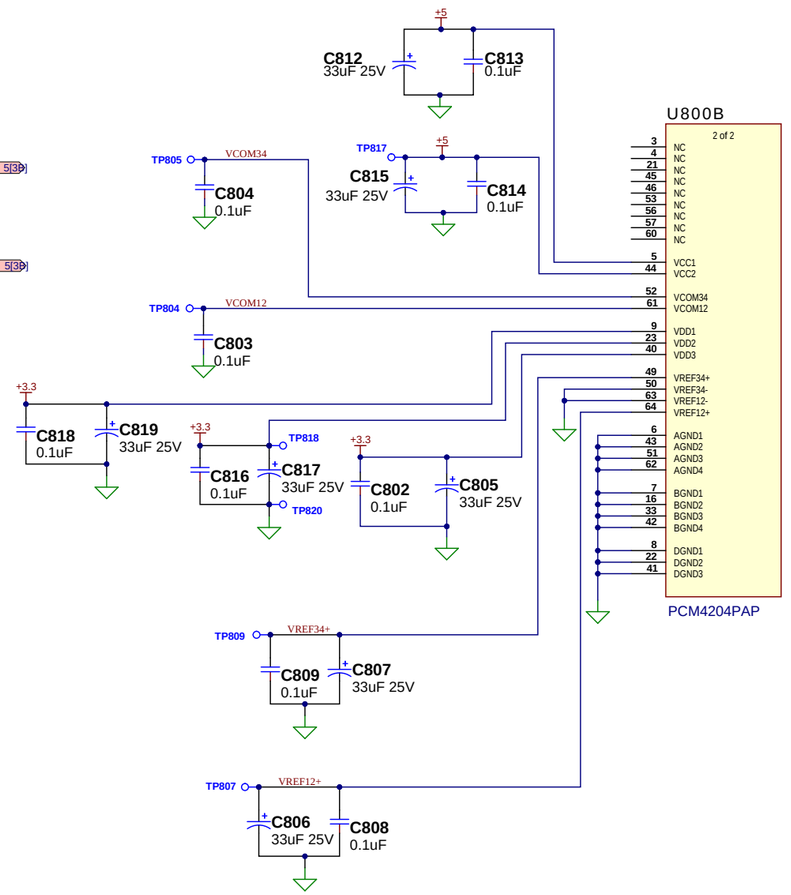






DNI by default so that VCOM is sourced from +5 rather than ADC

In 2-channel amps, VCOM2, not VCOM1, is used for AFE reference.



Change history for AKM-TI re-design – *this page only*

Change U800 ADC: AK5388AEQ to PCM4204PAPR

Remove C802, C805 (2.2µF) from VCOM rails to match TI application guidance

Add C802, C805 (0.1µF and 33µF) for VDD3 (note, these are re-used reference designators)

Change C812, C815, C817, C819 from 10µF to 33µF to match TI application guidance

Rearrange resistors to match required HW configuration, add resistors to provide configuration options where desired, and change all option resistors to 0Ω

Change VCOM/VREF configuration to match TI application guidance and Redline/Inferno design, and change R800, R801 to 1.5KΩ

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Dwg # SD870280-0010			
Drawn By: B. Sennett, B. Zhao			
Variant: *[No Variations]*			
Project: *Peak2KW_AKM_TI_Redesign*			
Size C 2B	Sheet # 8 of 23	Date 6/18/2021 3:19:44 PM	Rev. C
8_ADC.SchDoc			

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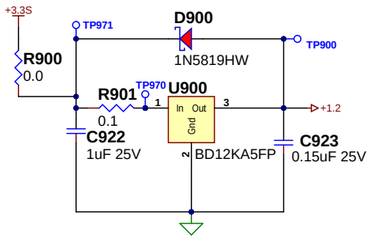
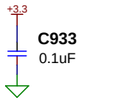
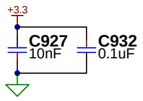
ADC

Linear regulator provides +1.2 to DSP

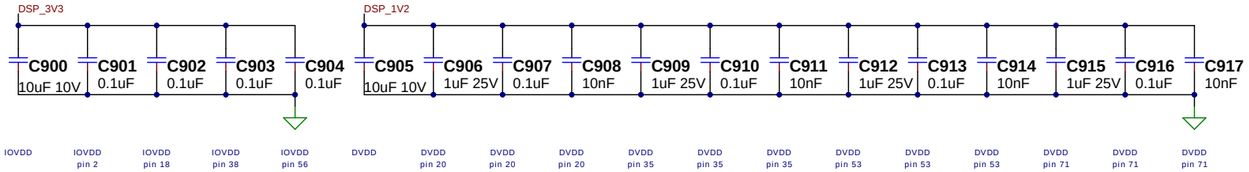


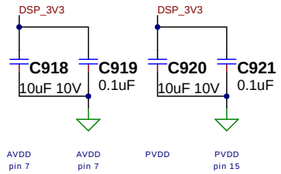


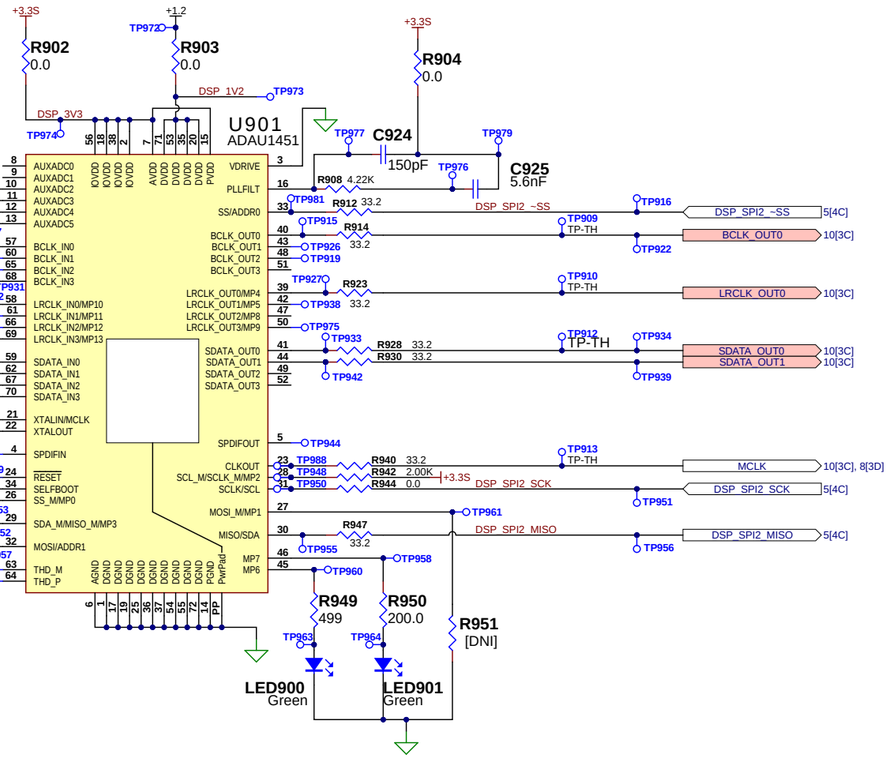
High-frequency bypass capacitor for layout.

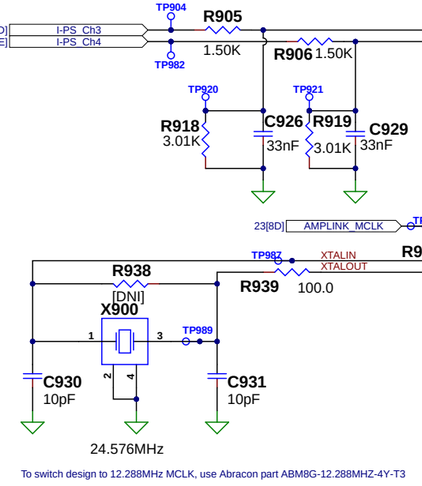


AC coupling caps to provide HF path from L3 plane



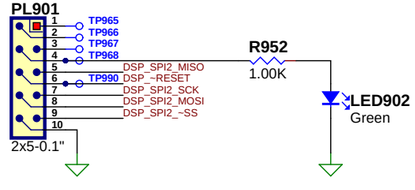






Ground test point to be placed as close as possible to TP901 and TP902 for measurement purposes.

To switch design to 12.288MHz MCLK, use Abracon part ABM8G-12.288MHZ-4Y-T3



ADAU1452 USBi Header

For connection to ADI EVAL-ADUSB2EBZ

Digital Audio Buses

Path	Bit Clock	Frame Clock	Audio Data	Clock Master
ADC > DSP	BCLK_IN0	LRCLK_IN0	SDATA_IN0 SDATA_IN1	DSP
DSP > DAC	BCLK_OUT0	LRCLK_OUT0	SDATA_OUT0 SDATA_OUT1	DSP
AmpLink > DSP	BCLK_IN3	LRCLK_IN3	SDATA_IN2 SDATA_IN3	AmpLink (XMOS)

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Dwg # SD870280-0010

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Drawn By: B. Sennett, B. Zhao

Variant: *[No Variations]*

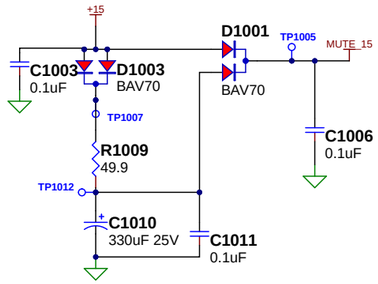
Project: *Peak2KW_AKM_TI_Redesign*

Size	Sheet #	Date	Rev.
C2B	9 of 23	6/18/2021 3:19:44 PM	C

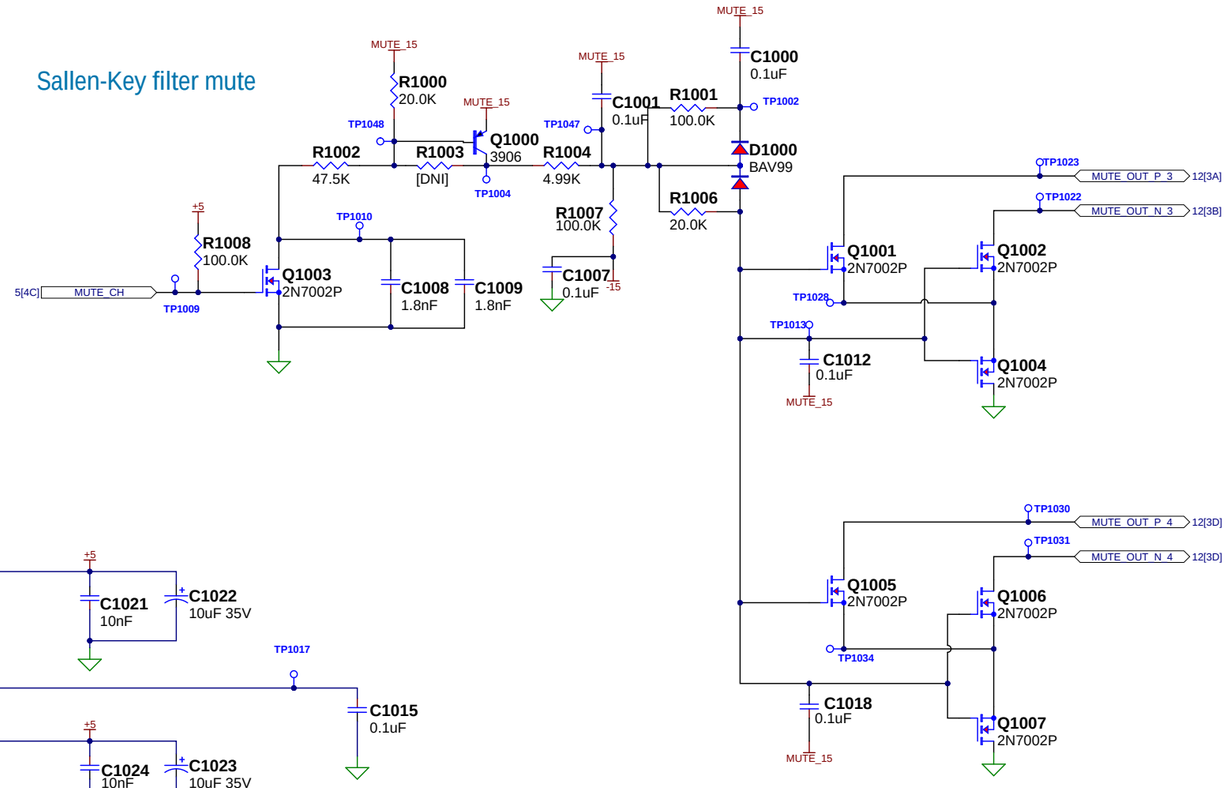
9_DSP.SchDoc

DSP

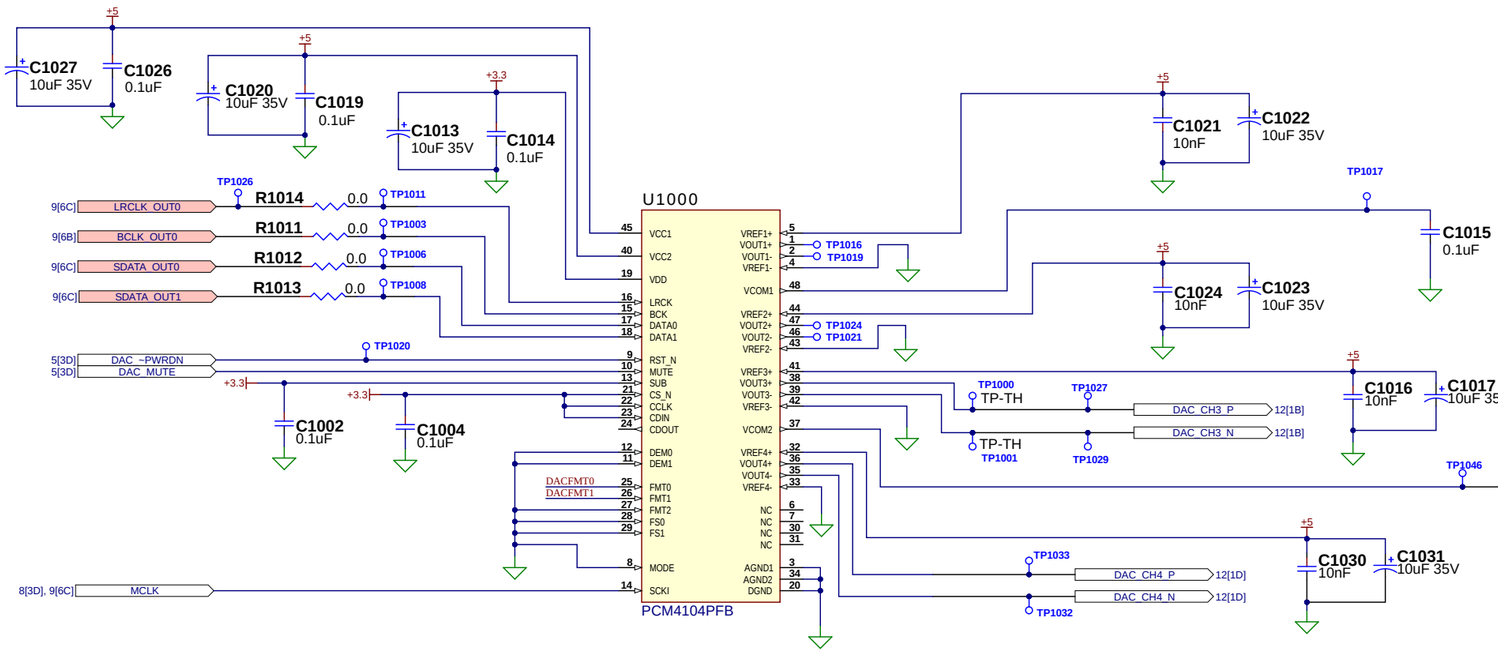
Mute power supply

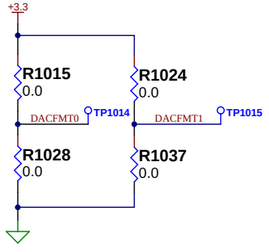


Sallen-Key filter mute



Digital-to-analog converter





DAC Option Configuration

ADC Pin	Signal Name	Setting	Configuration
8	MODE	LOW	Standalone mode
11	DEM1	LOW	De-emphasis filter off
12	DEM0	LOW	
13	SUB	HIGH	TDM sub-frame 1 (N/A)
25	FMT0	LOW	24-bit left-justified
26	FMT1	LOW	
27	FMT2	LOW	
28	FS0	LOW	Single rate (Fs = 48 kHz, SCKI
29	FS1	LOW	= 512Fs = 24.576 MHz)

Change history for AKM-TI re-design *– this page only*

Change U1000 DAC: AK4413EQ to PCM4104PFBR

Change C1022, C1023 from 100µF to 10µF to match TI application guidance

Change C1021, C1024 from 0.1µF to 10nF X7R to match TI application guidance

Add new VREF caps C1016, C1017, C1031, C1030 (note, these are re-used reference designators)

Remove R1010, R1027 (1MΩ cap discharge resistors)

Change C1015, C1028 from 10µF to 0.1µF to match TI application guidance

Remove C1032 (from assorted caps on +3.3 rail for previous DVDD supply; the other caps' designators were re-used)

Set configuration pins by tying to rails and set SPI input pins high.

Repurpose R1015, R1028 and R1024, R1037 pull-up/down pairs for FMT0/FMT1 to allow TDM configuration if needed. (FMT2 is tied since it only is used for Right-Justified configuration.)

Remove TP1025 (was on NC pin on previous DAC).

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Dwg # **SD870280-0010**

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Fax: (508) 820-9522

Drawn By: **B. Sennett**
B. Zhao

Variant: *[No Variations]*

Project: ***Peak2KW_AKM_TI_Redesign***

Size	Sheet #	Date	Rev.
C 2B	10 of 23	6/18/2021 3:19:44 PM	C

10_DAC.SchDoc

DAC and Power-Down Mute

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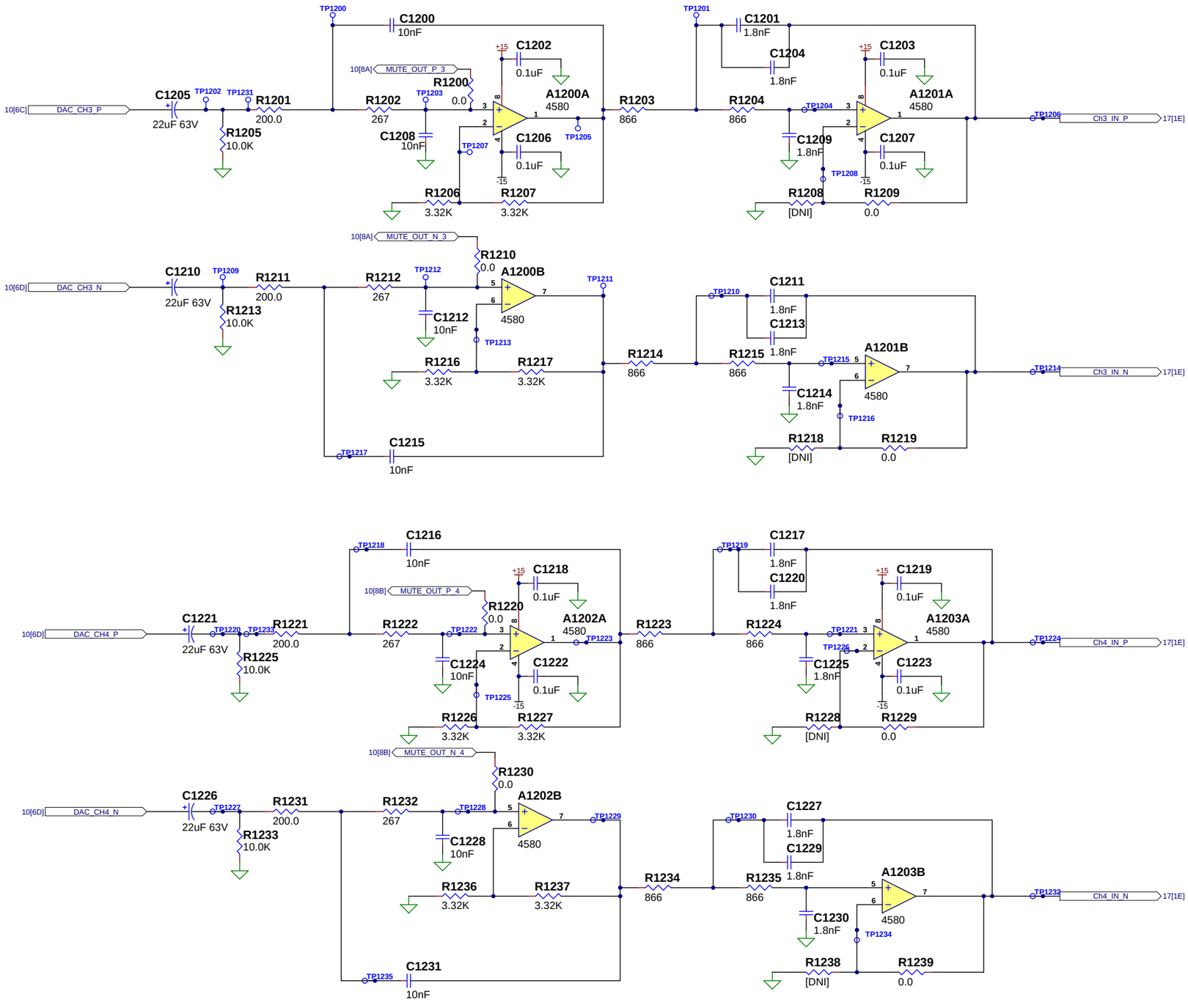
Size	Sheet #	Date	Rev.
C2B	11 of 23	6/18/2021 3:19:45 PM	C

11_SallenKey12.SchDoc

Sallen-Key Filters Ch. 1 & 2



BOSE PROFESSIONAL	Dwg # SD870280-0010	©Bose Corporation 145 Pennsylvania Ave. M/S 234 Framingham, MA 01701 (508) 766-5733 Fax: (508) 820-9522	
	Drawn By: B. Zhao		
	Variant: *[No Variations]*		
	Project: *Peak2KW_AKM_TI_Redesign*		
	Size C 2B	Sheet # 12 of 23	Date 6/18/2021 3:19:45 PM
	12_SallenKey34.SchDoc		Rev. C

Sallen-Key Filters Ch. 3 & 4

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Dwg # SD870280-0010		©Bose Corporation 145 Pennsylvania Ave. M/S 234 Framingham, MA 01701 (508) 766-4173 Fax: (508) 820-9522
Drawn By: Z. Coric D. Pearce		
Variant: *[No Variations]*		
Project: *Peak2KW_AKM_TI_Redesign*		
Size C2B	Sheet # 13 of 23 13_I-Share_Amp-Controller 1+2.SchDoc	Date 6/18/2021 3:19:45 PM Rev. C

Ch1&2 Controller & Interface

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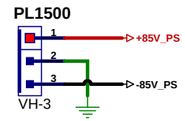
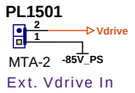
Dwg #	SD870280-0010
Drawn By:	Z. Coric D. Pearce
Variant:	*[No Variations]*
Project:	*Peak2KW_AKM_TI_Redesign*
Size	C 2B
Sheet #	14 of 23
Date	6/18/2021 3:19:45 PM
	14_I-Share_Amp-Controller-1+2-Page2.SchDoc
Rev.	C

Controller-Page2

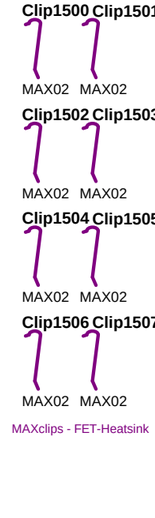


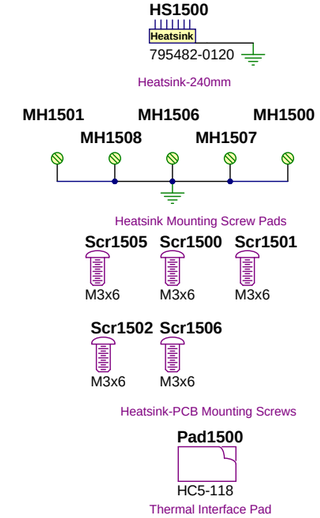


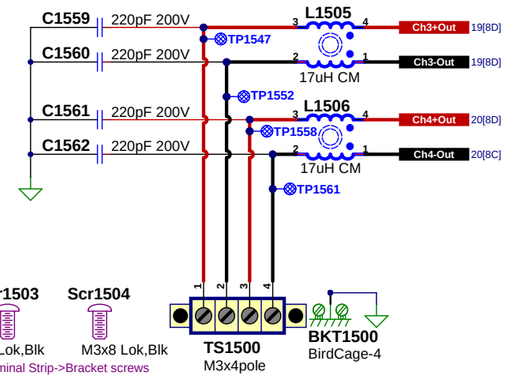
Note:

For 2-channel amps, Channels 3 & 4 are used. Common components are preserved.

The power connectors, output terminal strip, and amp heatsink hardware is shown on this page, but the remaining amp circuits are on Pages 17-20.







UNLESS OTHERWISE MARKED:

All Capacitors in µF, 50VDC

All Resistors 1/10W 1% Thick Film 0603

* Denotes part mounted on Heatsink

BOSE PROFESSIONAL

Dwg # **SD870280-0010**

Drawn By: **Z. Coric**
D. Pearce

Variant: ***[No Variations]***

Project: ***Peak2KW_AKM_TI_Redesign***

Size **C 2B** | Sheet # **15** of **23** | Date **6/18/2021** 3:19:45 PM | Rev. **C**

15_Ch1 Drive+Output_I-Share.SchDoc

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Ch1 Driver & Output Stage

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Dwg # SD870280-0010

Drawn By: Z. Coric
D. Pearce

Variant: *[No Variations]*

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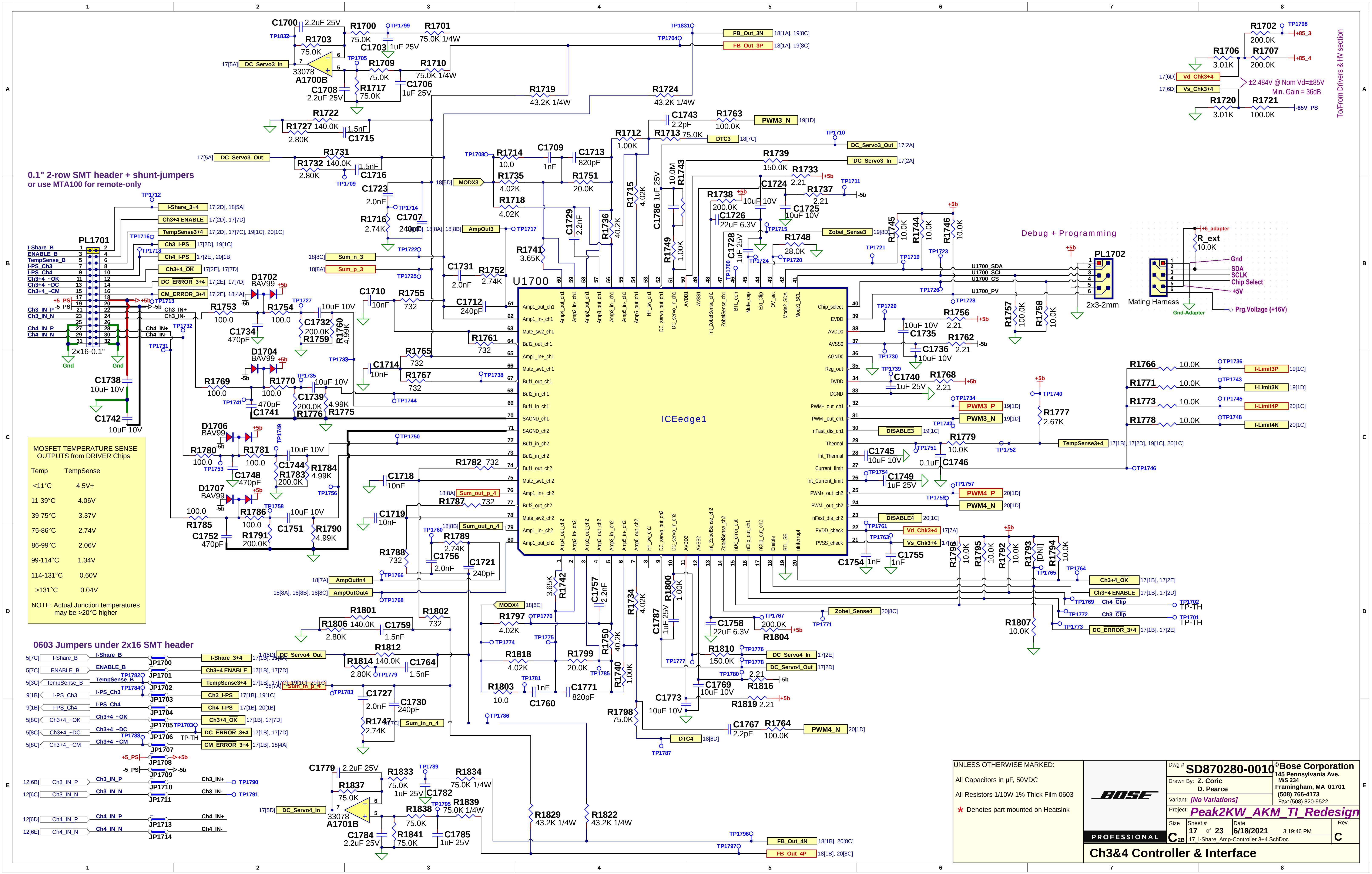
Project: *Peak2KW_AKM_TI_Redesign*

Size	Sheet #	Date	Rev.
C2B	16 of 23	6/18/2021 3:19:45 PM	C

16_Ch2 Drive+Output_I-Share.SchDoc

Ch2 Driver + Output Stage


0.1" 2-row SMT header + shunt-jumpers
or use MTA100 for remote-only
PL1701
2x16-0.1"
MOSFET TEMPERATURE SENSE OUTPUTS from DRIVER Chips
Temp TempSense
<11°C 4.5V+
11-39°C 4.06V
39-75°C 3.37V
75-86°C 2.74V
86-99°C 2.06V
99-114°C 1.34V
114-131°C 0.60V
>131°C 0.04V
NOTE: Actual Junction temperatures may be >20°C higher
0603 Jumpers under 2x16 SMT header
U1700
ICEedge1
A1700B
A1701B
Debug + Programming
PL1702
2x3-2mm
Mating Harness
±2.484V @ Nom Vd=±85V
Min. Gain = 36dB
To/From Drivers & HV section
UNLESS OTHERWISE MARKED:
All Capacitors in µF, 50VDC
All Resistors 1/10W 1% Thick Film 0603
* Denotes part mounted on Heatsink
BOSE PROFESSIONAL
Dwg # SD870280-0010
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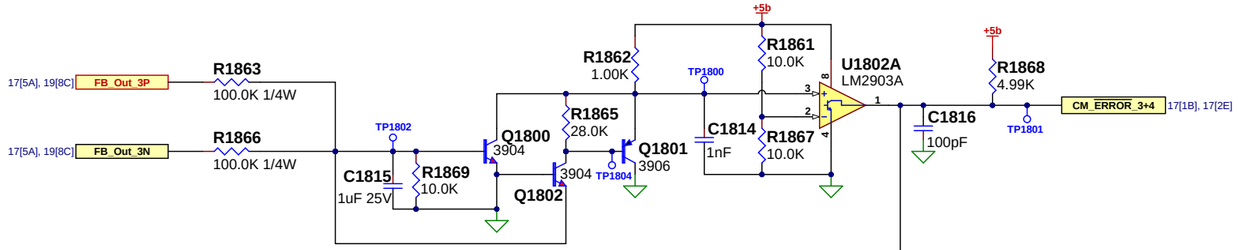
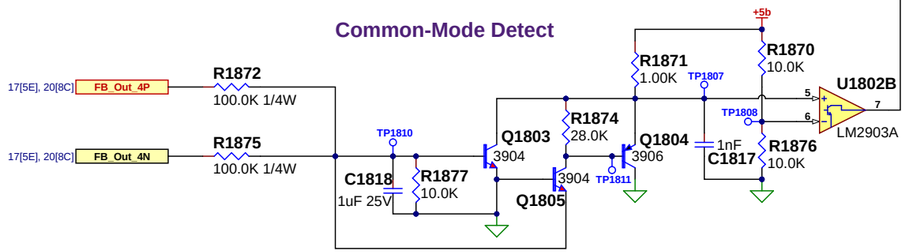
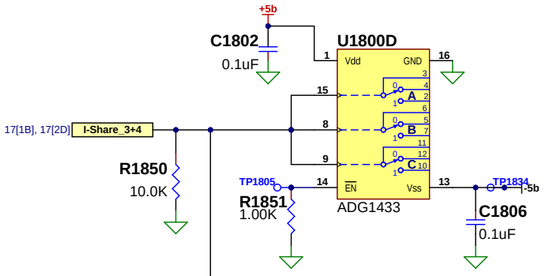
Fax: (508) 820-9522
Drawn By: Z. Coric
D. Pearce
Variant: [No Variations]
Project: Peak2KW_AKM_TI_Redesign
Size C2B
Sheet # 17 of 23
Date 6/18/2021 3:19:46 PM
17_I-Share_Amp-Controller 3+4.SchDoc
Rev. C
Ch3&4 Controller & Interface

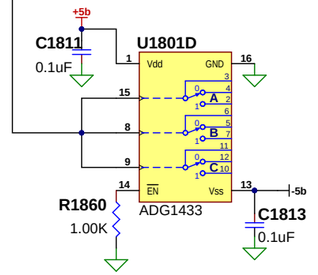


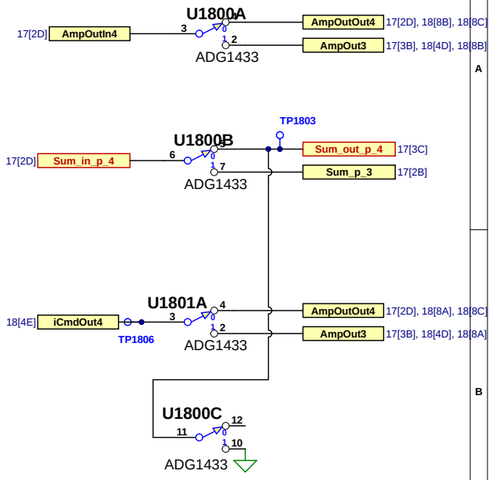
Common-Mode Detect

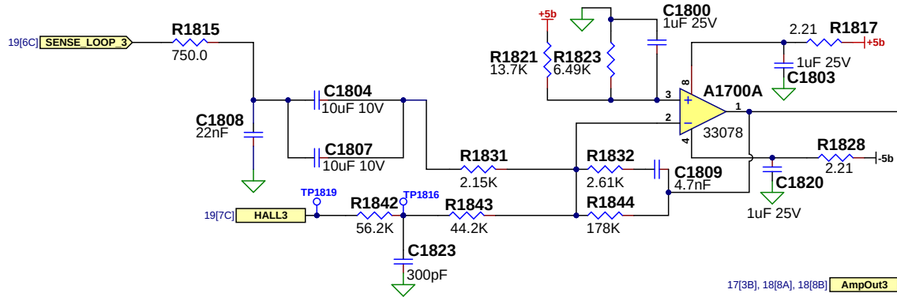


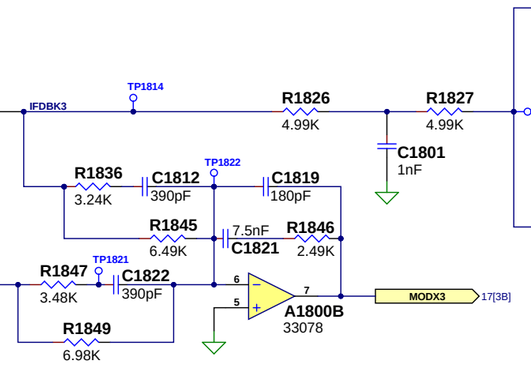


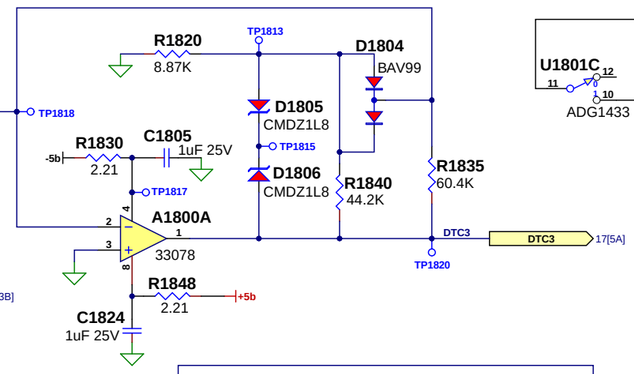
I-Share Signal Routing

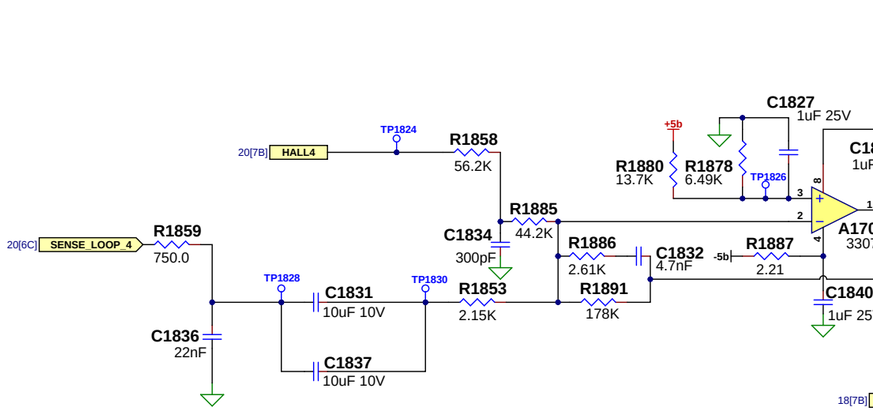


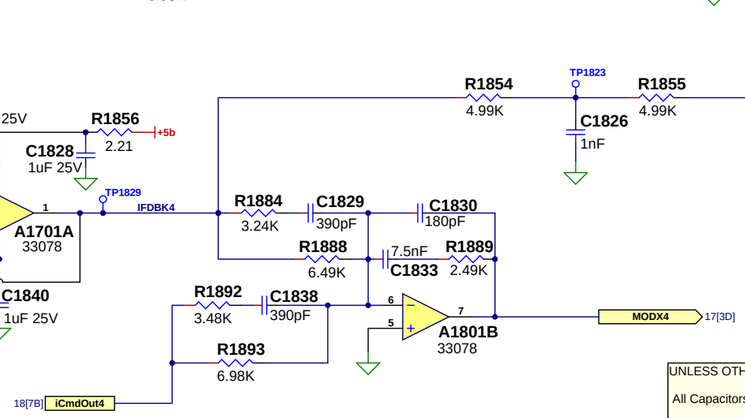


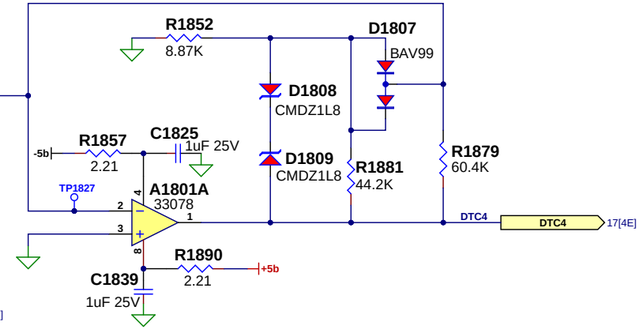












UNLESS OTHERWISE MARKED:

All Capacitors in µF, 50VDC

All Resistors 1/10W 1% Thick Film 0603

* Denotes part mounted on Heatsink

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Dwg #	SD870280-0010
Drawn By:	Z. Coric, D. Pearce
Variant:	[No Variations]
Project:	Peak2KW_AKM_TI_Redesign
Size	C2B
Sheet #	18 of 23
Date	6/18/2021 3:19:46 PM
Rev.	C
File	18_I-Share_Amp-Controller 3+4_Page2.SchDoc

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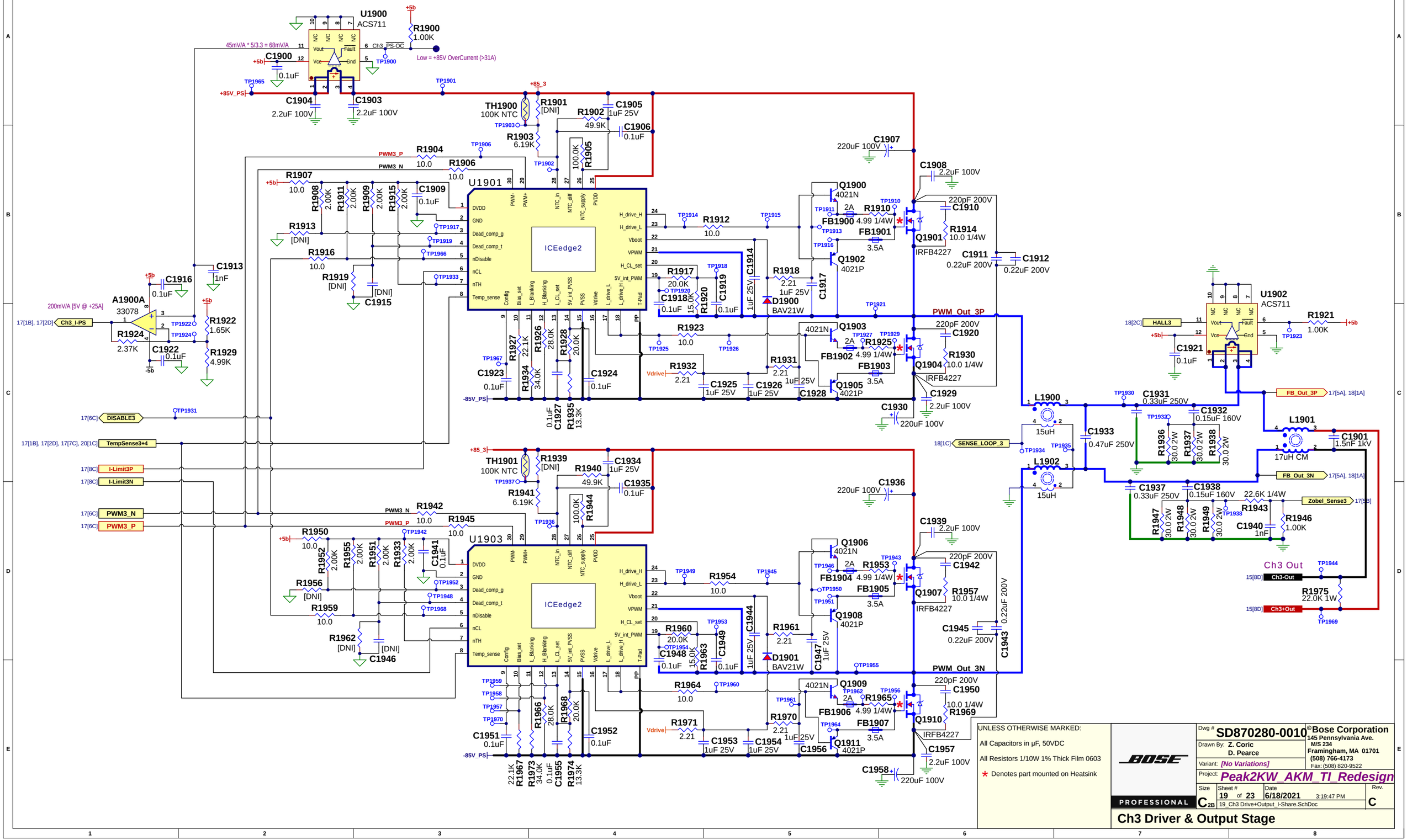
Controller-Page2


U1900
ACS711
R1900
1.00K
+5b
45mV/A * 5/3.3 = 68mV/A
C1900
0.1uF
Ch3_PS-OC
TP1900
Low = +85V OverCurrent (>31A)
TP1965
+85V_PS
C1904
2.2uF 100V
C1903
2.2uF 100V
TP1901
+85_3
TH1900
100K NTC
TP1903
R1901
[DNI]
R1902
49.9K
C1905
1uF 25V
C1906
0.1uF
R1903
6.19K
R1905
100.0K
TP1902
TP1906
PWM3_P
PWM3_N
R1904
10.0
R1906
10.0
U1901
ICEedge2
DVDD
GND
Dead_comp_g
Dead_comp_t
nDisable
nCL
nTH
Temp_sense
PWM-
PWM+
NTC_in
NTC_diff
NTC_supply
PVDD
H_drive_H
H_drive_L
Vboot
VPWM
H_CL_set
5V_int_PWM
T-Pad
R1907
10.0
R1908
2.00K
R1911
2.00K
R1909
2.00K
R1915
2.00K
C1909
0.1uF
R1913
[DNI]
R1916
10.0
R1919
[DNI]
C1915
TP1917
TP1919
TP1966
TP1933
C1913
1nF
C1916
0.1uF
A1900A
33078
200mV/A [5V @ +25A]
17[1B], 17[2D]
Ch3_I-PS
TP1922
TP1924
R1924
2.37K
C1922
0.1uF
R1922
1.65K
R1929
4.99K
-5b
17[6C]
DISABLE3
TP1931
17[1B], 17[2D], 17[7C], 20[1C]
TempSense3+4
17[8C]
I-Limit3P
17[8C]
I-Limit3N
17[6C]
PWM3_N
17[6C]
PWM3_P
R1912
10.0
TP1914
TP1915
Q1900
4021N
TP1911
2A
R1910
4.99 1/4W
FB1900
FB1901
3.5A
TP1913
TP1916
Q1902
4021P
R1917
20.0K
TP1918
TP1920
C1918
0.1uF
R1920
15.0K
C1919
0.1uF
C1914
1uF 25V
R1918
2.21
1uF 25V
C1917
D1900
BAV21W
TP1921
C1907
220uF 100V
C1908
2.2uF 100V
Q1901
IRFB4227
220pF 200V
C1910
R1914
10.0 1/4W
C1911
0.22uF 200V
C1912
0.22uF 200V
PWM_Out_3P
R1923
10.0
TP1925
TP1926
Q1903
4021N
TP1927
TP1929
R1925
4.99 1/4W
FB1902
FB1903
3.5A
Q1904
IRFB4227
220pF 200V
C1920
R1930
10.0 1/4W
R1927
22.1K
R1926
28.0K
R1928
20.0K
TP1967
C1923
0.1uF
C1924
0.1uF
R1934
34.0K
C1927
0.1uF
R1935
13.3K
-85V_PS
R1932
2.21
Vdrive
C1925
1uF 25V
C1926
1uF 25V
R1931
2.21
1uF 25V
C1928
Q1905
4021P
C1929
2.2uF 100V
C1930
220uF 100V
U1902
ACS711
18[2C]
HALL3
R1921
1.00K
C1921
0.1uF
TP1923
FB_Out_3P
17[5A], 18[1A]
L1900
15uH
TP1930
C1931
0.33uF 250V
C1932
0.15uF 160V
L1901
17uH CM
C1901
1.5nF 1kV
FB_Out_3N
17[5A], 18[1A]
C1933
0.47uF 250V
18[1C]
SENSE_LOOP_3
TP1934
TP1935
L1902
15uH
TP1932
R1936
30.0 2W
R1937
30.0 2W
R1938
30.0 2W
C1937
0.33uF 250V
C1938
0.15uF 160V
22.6K 1/4W
Zobel_Sense3
17[5B]
R1947
30.0 2W
R1948
30.0 2W
R1949
30.0 2W
TP1938
R1943
R1946
1.00K
C1940
1nF
Ch3 Out
TP1944
15[8D]
Ch3-Out
R1975
22.0K 1W
15[8D]
Ch3+Out
TP1969
TH1901
100K NTC
TP1937
R1939
[DNI]
R1940
49.9K
C1934
1uF 25V
C1935
0.1uF
R1941
6.19K
R1944
100.0K
TP1936
PWM3_N
PWM3_P
R1942
10.0
R1945
10.0
U1903
ICEedge2
R1950
10.0
R1952
2.00K
R1955
2.00K
R1951
2.00K
R1933
2.00K
C1941
0.1uF
R1956
[DNI]
R1959
10.0
R1962
[DNI]
C1946
TP1952
TP1948
TP1968
R1954
10.0
TP1949
TP1945
Q1906
4021N
TP1946
2A
R1953
4.99 1/4W
FB1904
FB1905
3.5A
TP1950
TP1951
Q1908
4021P
R1960
20.0K
TP1953
TP1954
C1948
0.1uF
R1963
15.0K
C1949
0.1uF
C1944
1uF 25V
R1961
2.21
1uF 25V
C1947
D1901
BAV21W
TP1955
C1936
220uF 100V
C1939
2.2uF 100V
Q1907
IRFB4227
220pF 200V
C1942
R1957
10.0 1/4W
C1945
0.22uF 200V
C1943
0.22uF 200V
PWM_Out_3N
R1964
10.0
TP1960
TP1959
TP1958
TP1957
TP1970
Q1909
4021N
TP1962
TP1956
2A
R1965
4.99 1/4W
FB1906
FB1907
3.5A
Q1910
IRFB4227
220pF 200V
C1950
10.0 1/4W
R1969
TP1961
R1966
28.0K
R1968
20.0K
C1951
0.1uF
C1952
0.1uF
R1970
2.21
1uF 25V
C1956
R1971
2.21
Vdrive
C1953
1uF 25V
C1954
1uF 25V
Q1911
4021P
C1957
2.2uF 100V
C1958
220uF 100V
R1967
22.1K
R1973
34.0K
C1955
0.1uF
R1974
13.3K
-85V_PS
UNLESS OTHERWISE MARKED:
All Capacitors in µF, 50VDC
All Resistors 1/10W 1% Thick Film 0603
* Denotes part mounted on Heatsink
BOSE
PROFESSIONAL
Dwg # SD870280-0010
Drawn By: Z. Coric
D. Pearce
Variant: [No Variations]
Project: Peak2KW_AKM_TI_Redesign
Size C2B
Sheet # 19 of 23
Date 6/18/2021 3:19:47 PM
Rev. C
19_Ch3 Drive+Output_I-Share.SchDoc
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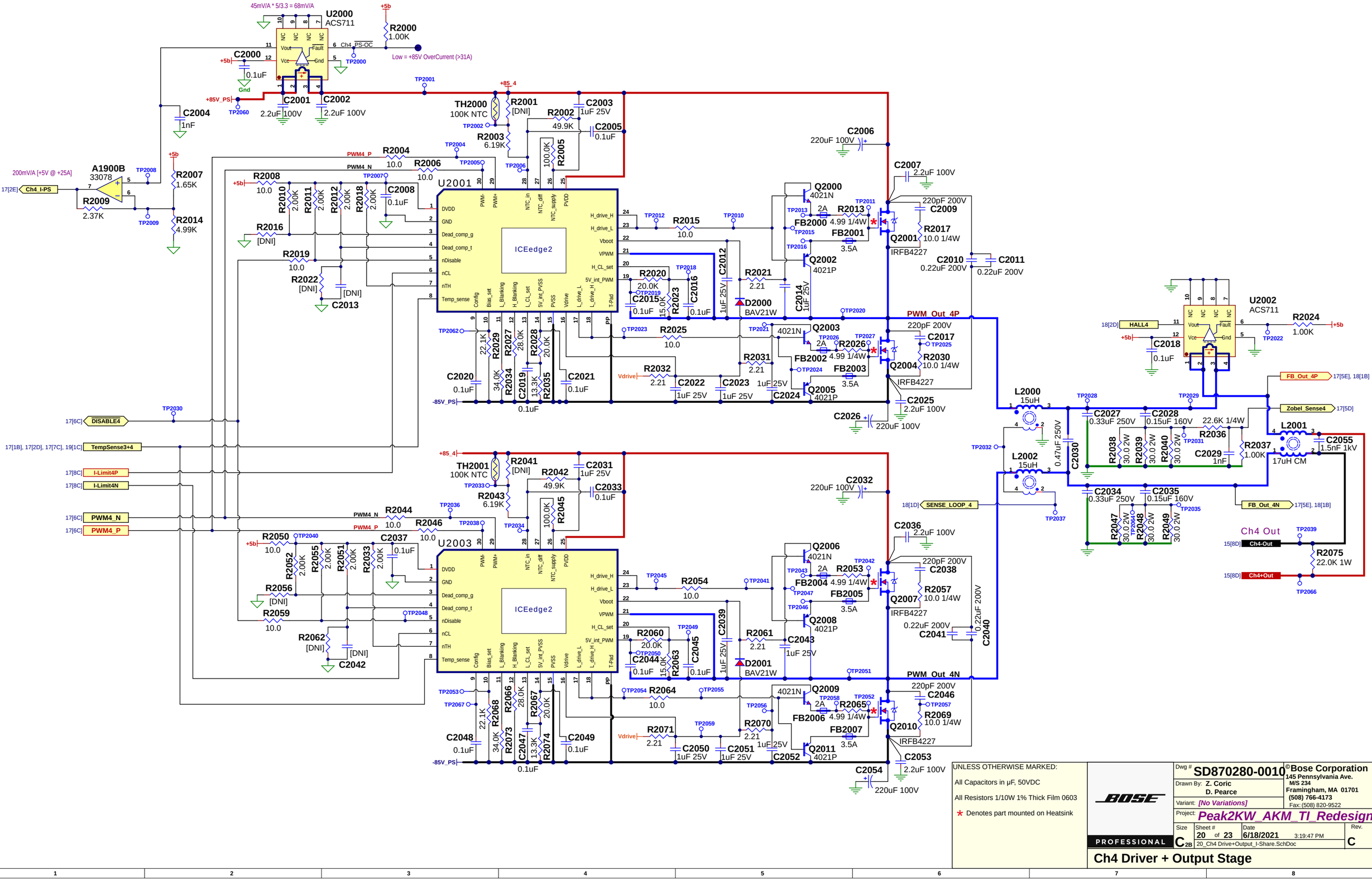
Ch3 Driver & Output Stage



UNLESS OTHERWISE MARKED:

All Capacitors in µF, 50VDC

All Resistors 1/10W 1% Thick Film 0603

* Denotes part mounted on Heatsink

BOSE PROFESSIONAL

Dwg # SD870280-0010

145 Pennsylvania Ave.
M/S 234
Framingham, MA 01701
(508) 766-4173
Fax: (508) 820-9522

Drawn By: Z. Coric, D. Pearce

Variant: *[No Variations]*

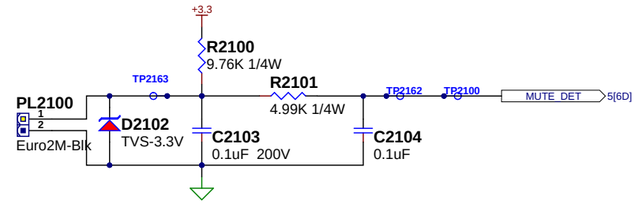
Project: *Peak2KW_AKM_TI_Redesign*

Size	Sheet #	Date	Rev.
C2B	20 of 23	6/18/2021 3:19:47 PM	C

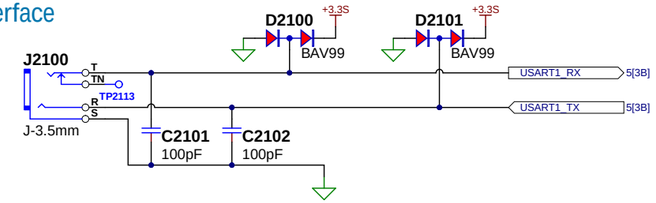
20_Ch4 Drive+Output_I-Share.SchDoc

Ch4 Driver + Output Stage

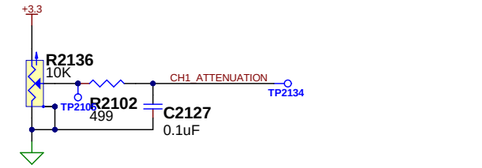
Mute connector



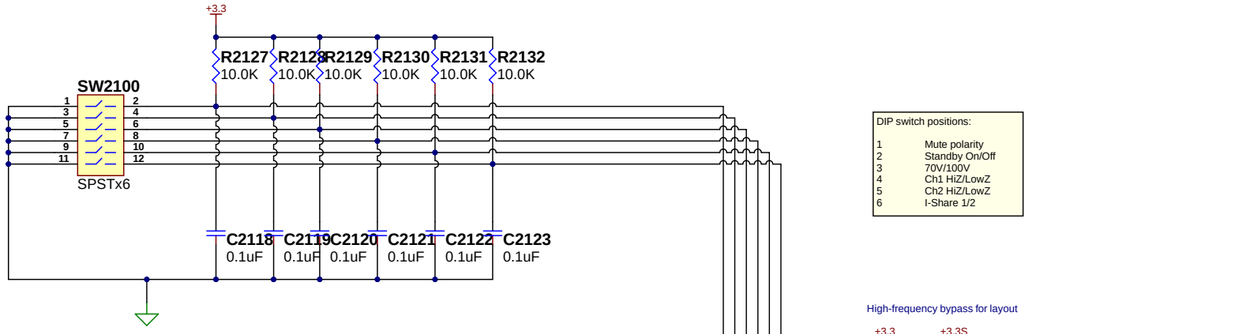
Factory UART interface



Attenuators



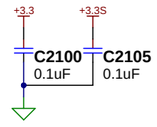
DIP switches



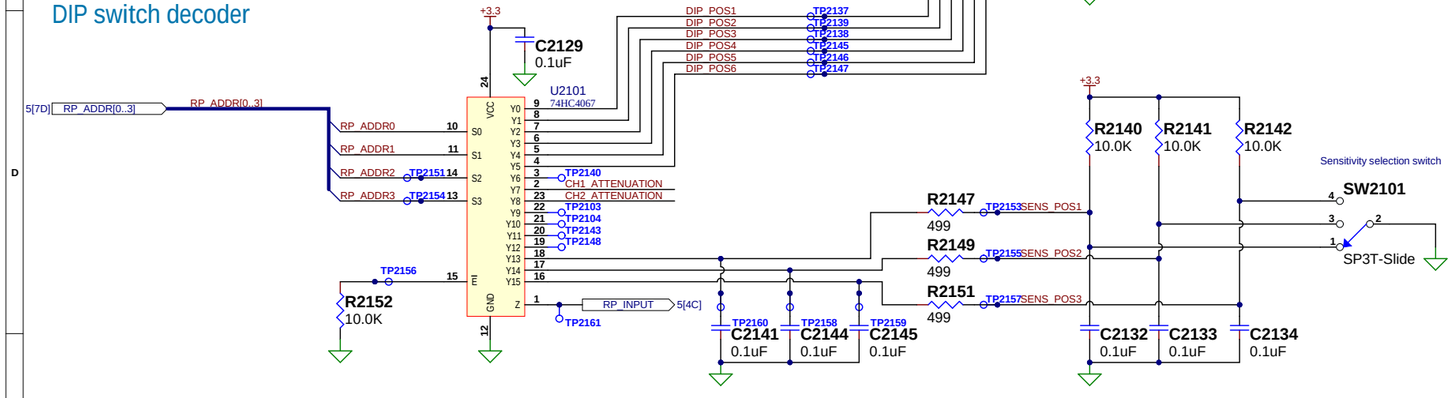
DIP switch positions:

1	Mute polarity
2	Standby On/Off
3	70V/100V
4	Ch1 HiZ/LowZ
5	Ch2 HiZ/LowZ
6	I-Share 1/2

High-frequency bypass for layout

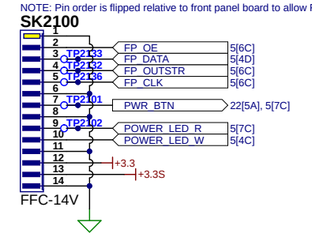


DIP switch decoder

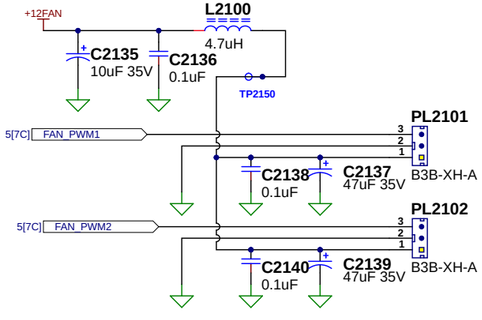


Front panel connector

NOTE: Pin order is flipped relative to front panel board to allow FFC to be straight.



Fan connectors



145 Pennsylvania Ave.
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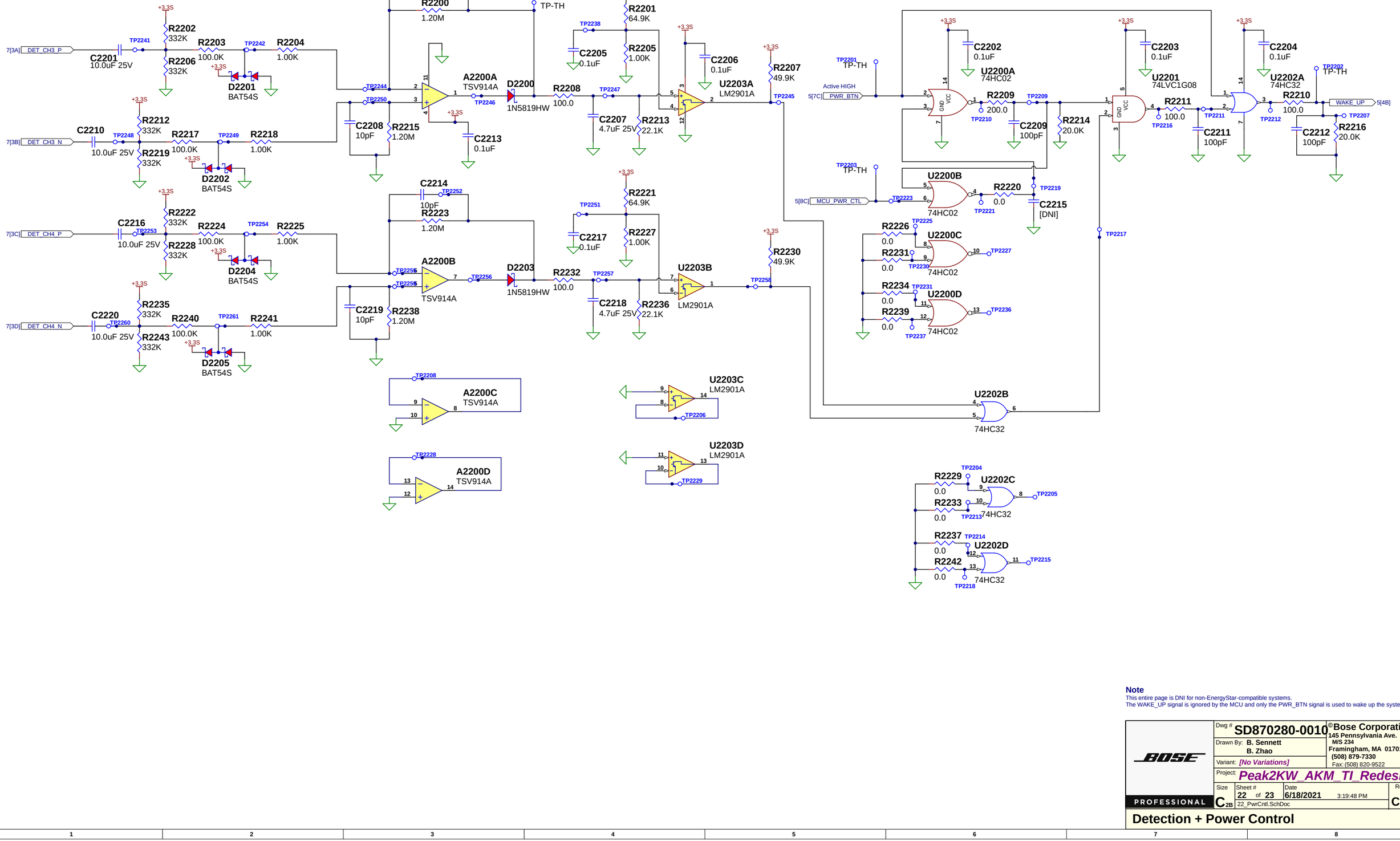
Fax: (508) 820-9522

Dwg #	SD870280-0010
Drawn By:	B. Sennett, B. Zhao
Variant:	[No Variations]
Project:	Peak2KW_AKM_TI_Redesign
Size	C2B
Sheet #	21 of 23
Date	6/18/2021 3:19:47 PM
Rev.	C
	21_RearPanel.SchDoc

PROFESSIONAL

Rear-Panel Features, Connectors



Note
This entire page is DNI for non-EnergyStar-compatible systems.
The WAKE_UP signal is ignored by the MCU and only the PWR_BTN signal is used to wake up the system.

PROFESSIONAL	Dwg # SD870280-0010	©Bose Corporation 145 Pennsylvania Ave. M/S 234 Framingham, MA 01701 (508) 879-7330 Fax: (508) 820-9522
	Drawn By: B. Sennett B. Zhao	
	Variant: *[No Variations]*	
	Project: *Peak2KW_AKM_TI_Redesign*	
	Size C2B · Sheet # 22 of 23 · Date 6/18/2021 3:19:48 PM · Rev. C	
	22_PwrCntl.SchDoc	

Detection + Power Control

Input and Thru RJ45 jacks

LVDS protection, magnetics, transceivers

XMOS processor

Clocking and PLL

Rotary input selector

XMOS programming/debug header

XMOS outboard flash

XMOS power and reset controller

XMOS processor 1.0V supply decoupling caps - place close to pins indicated

XMOS processor 3.3V supply decoupling caps - place close to pins indicated

Bypass caps for EMI on 24.576MHz clocks

ADAT input selection	
DSW_ADATx	Enable
0	0
1	1
2	2

Compile version selection	
A1/A0	Channels
00	2
01	4
10	8
11	Reserved

Data format: 0 = I2S; 1 = MSB (left justified)
Sample rate: 0 = 48 kHz; 1 = 96 kHz

To switch design to 12.288MHz MCLK, use SiTime part SIT8008BC-82-33E-12.288000X

Dwg #	SD870280-0010
Drawn By:	B. Sennett
Variant:	[No Variations]
Project:	Peak2KW_AKM_TI_Redesign
Size	C2B
Sheet #	23 of 23
Date	6/18/2021 3:19:48 PM
Rev.	C
	23_AmpLink.SchDoc

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AmpLink Digital Input